ABSTRACT OF THE DISCLOSURE

A semiconductor device comprises a semiconductor substrate including an isolation region defining an active area with a plurality of source/drain regions. A contact pad layer is formed on the semiconductor substrate and includes gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions. A first interlevel dielectric layer covers the gate line structures and the first and second contact pads. A bit line contact plug layer is formed on the contact pad layer and includes lower storage node contact plugs connected to the first contact pads, bit line contact plugs connected to the second contact pads. A protective layer pattern is formed on the second contact pads to prevent the second contact pads from being connected to the lower storage node contact plugs and/or upper storage node contact plugs.